HAILO

Empowering Intelligence

Hailo-8L Datasheet

Revision 1.9.3

April 2026

Part Number

Industrial: HNC1LBI11BH

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Documentation Control

History Table

Revision	Date	Description
0.1	July 2022	First preliminary release
1.0	November 2022	Removal of commercial part details
1.1	December 2022	Section 2.2-U5 removed from GND Replaced V3 with A19 Section 2.2 U5 and J3 added to RESERVED
1.2	August 2023	Updated voltages in Section 4.2 Recommended Operating Conditions Revised Section 4.3 Power-up Sequence New sequence description, drawing and timing requirements table
1.3	October 2023	Updated system modes and usage scenarios
1.4	December 2023	Section 4.4.1 updated VDDIO to 300 mA, Max VDD_Core to 7.2A and Max VDD_Top to 1A Typo correction on pin names PCIE_REFCLK and CSI_TX _CLK
1.5	August 2024	Updated Functional Assignment table
1.6	April 2025	Updated power rail voltage values Section 4.1.1
1.7	August 2025	Maximum PCIe payload for Hailo-8L is 256 Byte
1.9	January 2026	Revised datasheet
1.9.1	February 2026	Added V04, V06, V10 and U04 to the Functional Assignment table
1.9.2	March 2026	Added H19, H20, M19, M20 and V12 to the Functional Assignment table
1.9.3	April 2026	Updated the power modes data in Section 5.3 NN Core

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Glossary

Table 1 provides a useful list of acronyms and abbreviations.

Table 1. Glossary of terms

Abbreviation	Definition
CMOS	Complementary Metal-Oxide Semiconductor
CS	Chip Select
DMA	Direct Memory Access
DNN	Deep Neural Network
ECC	Error Correction Code
FPS	Frames per Second
FPU	Floating Point Accelerator Unit
GND	Ground
GPIO	General-Purpose Input Output
HS	High Speed
I/O	Input Output
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LVCMOS	Low Voltage CMOS (Technology)
MCU	Microcontroller Unit
MMU	Memory Management Unit
MPU	Memory Protection Unit
NN	Neural Network
PCIe	Peripheral Component Interconnect Express
PHY	Physical Layer
PLL	Phase-Locked Loop
PVT	Process, Voltage, and Temperature
QSPI	Quad Serial Peripheral Interface
SPI	Serial Peripheral Interface
TOPS	Tera Operations Per Second

Abbreviation	Definition
UART	Universal Asynchronous Receiver Transmitter
VCC	Supply Voltage to Circuit
VDD	Operating Voltage of the Chip
VDDIO	Operating Voltage for I/O Digital Interface

1. Overview

1.1. Introduction

This datasheet provides a technical description of the Hailo-8L Artificial Intelligence (AI) accelerator and guidelines for proper design with the Hailo-8L. This document should be used in conjunction with the Hailo-8L Board Design Guidelines

The Hailo-8L shares the same innovative architecture and core features as the Hailo-8, while offering a lower performance grade optimized for applications that prioritize cost and power over peak performance. Despite this optimization, the Hailo-8L delivers industry-leading NN compute capability at the target operating point, with exceptional TOPS/W efficiency.

1.2. General Description

The Hailo-8L delivers high efficiency for neural network (NN) deployment through unique architecture elements within its NN Core, including:

- **A distributed memory fabric with purpose-built pipeline** elements that enable extremely low-power memory access during NN processing.
- **Highly efficient computational** elements that can be flexibility allocated based on workload requirements.
- **A dataflow-oriented interconnect** that adapts to the structure of the NN and enables high resource utilization.

The NN Core can be combined with multiple industry-leading interfaces and subsystems to deliver high efficiency and high compute, leading-edge AI solutions.

Hailo-8L integrates an optimal balance of performance, low power consumption, and advanced video analytics processing, enabling a wide range of AI-driven applications.

1.3. Applications

The Hailo-8L enables a broad range of applications, including:

- Smart cities: public safety, intelligent mobility, health monitoring, infrastructure & services management
- Industry 4.0: manufacturing automation, robotic vision, safety & security
- Smart retail: automated store, smart analytics, targeted advertising
- Smart home: lifestyle & entertainment, safety & security
- Drones: sensing, avoidance and navigation

1.4. Features

Neural Processing Unit (NN-Core)

- Hailo NN multi-stream, multi-network core up to 13 TOPS
- Hardware offload engines for Deep Neural Networks (DNN) with pre and post processing:
  - Tensor manipulation (crop & resize, ROI pooling, reshape)
  - Non Maximum Suppression (NMS)
  - Bi-linear transformation
  - Softmax

MCU

- Dual ARM Cortex-M4 processors @200MHz
- 640 KB internal SRAM (ECC protected)
- FPU, MPU

Interfaces

- 4-lane PCI Express Gen3 endpoint with integrated PHY
- 2 UART interfaces
- 4 I2C interfaces
- Quad SPI Interface
  - Supports clock rates up to 50MHz
  - Provides access to external serial flash devices for code and data storage

System Peripherals

- Voltage monitor
- Temperature sensor

Security features

- Hardware crypto accelerators
- Firewall
- Secure ROM and Boot

Package

- 400-pin HFCBGA
- 0.8mm pitch
- 17mm x 17mm

1.5. Block Diagram

The subsystems and functional modules of the Hailo-8L are displayed in Figure 1 below.

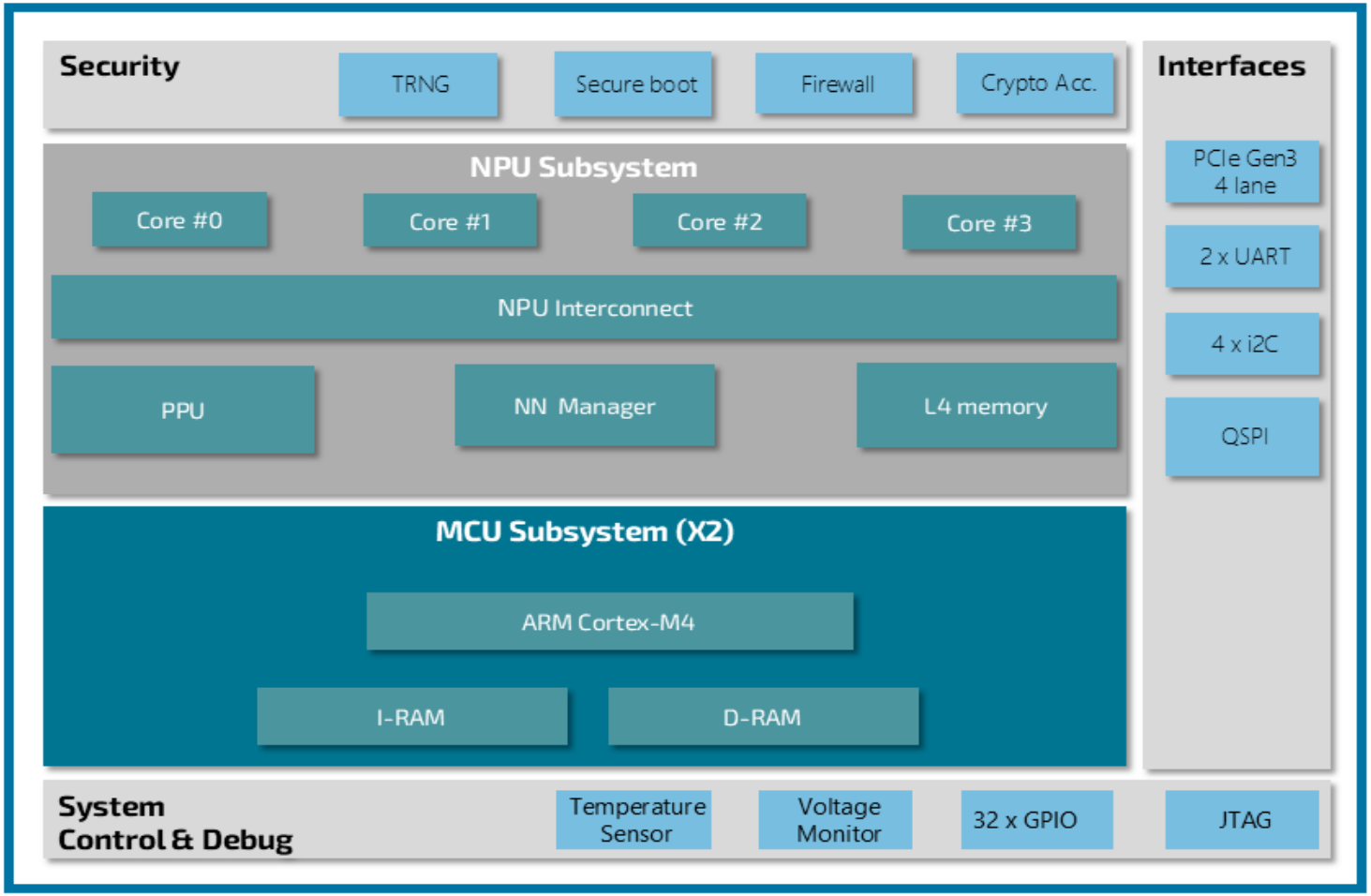

Figure 1. Hailo-8L block diagram

1.6. Ordering Information

Table 2. Part ordering information

Part Number	Device Grade	Operating Temperature Range
HNC1LBI11BH	Hailo-8L Industrial	-40 to 85 °C

The Hailo-8L device is shipped with the marking HNC1LBI11BH or HNC18BI11BH.

Refer to PCN-1002-01 in the Hailo Development Zone for more details.

1.7. Mechanical Details

The top, side and bottom views of the 400-pin HFCBGA package are displayed in Figure 2 and Table 3 lists the package dimensions.

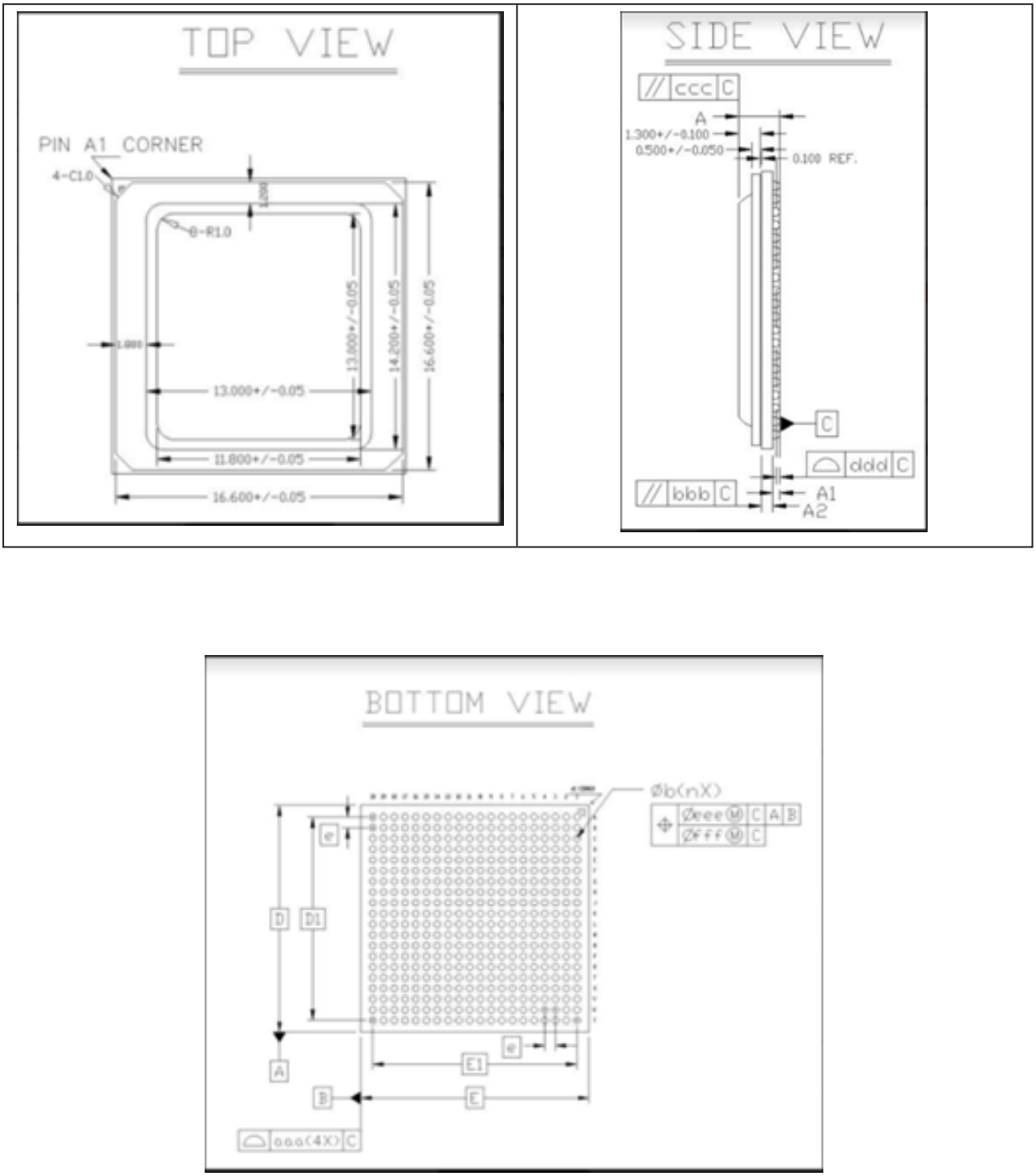

Figure 2. Hailo-8L package views

Table 3. Hailo-8L package dimensions

Description	Symbol	Common Dimensions		
		Min	Nom	Max
Total thickness	A	2.326	2.476	2.626
Stand-off	A1	0.300	-	0.500
Substrate thickness	A2	C676 Ref		
Body size	E	17 BSC		
	D	17 BSC		
Ball diameter		0.500		
Ball width	b	0.400	-	0.600
Ball pitch	e	C.800 BSC		
Ball count	d	400		
Edge ball center to center	E1	15.200 BSC		
	D1	15.200 BSC		
Package edge tolerance	aaa	C.200		
Substrate parallelism	bbb	C.250		
Top parallelism	ccc	C.350		
Coplanarity	ddd	0.150		
Ball offset (package)	eee	0.250		
Ball offset (ball)	fff	0.100		

2. Pinout Description

2.1. Pin Assignment

The two pin charts in Figure 3 show the pin layout and coordinate map for the Hailo-8L ball grid pin assignments.

	01	02	03	04	05	06	07	08	09	10
A	GND	NC	NC	PCIE_AVDD_C	GND	PCIE_TX0_P	PCIE_RX0_P	PCIE_TX1_P	PCIE_RX1_P	PCIE_REFCLK_P
B	NC	NC	NC	PCIE_AVDD_C	GND	PCIE_TX0_N	PCIE_RX0_N	PCIE_TX1_N	PCIE_RX1_N	PCIE_REFCLK_N
C	NC	NC	NC	GND	GND	PCIE_AVDD_D	PCIE_AVDD_D	PCIE_AVDD_D	GND	GND
D	GND	VDDIO	VDDIO	GND	GND	PCIE_WAKE_N	GND	PCIE_CLKREQ_N	PCIE_PERST_N	GND
E	NC	NC	NC	GND	GND	GND	GND	GND	GND	AVDD_TS
F	NC	NC	NC	GND	VDD	VDD	GND	GND	VDD	VDD
G	GND	GND	GND	GND	VDD	VDD	GND	GND	VDD	VDD
H	UART0_TXD	UART1_TXD	RSVD	GND	VDD	VDD	GND	GND	VDD	VDD
J	UART0_RXD	UART1_RXD	RSVD	VDD_SENSE	VDD	VDD	GND	GND	VDDIO	VDDIO
K	NC	GND	NC	GND	VDD	VDD	GND	GND	VDDIO	VDDIO
L	NC	GND	NC	AVDD_VS	VDD	VDD	GND	GND	VDD	VDD
M	GND	GND	GND	GND	VDD	VDD	GND	GND	VDD	VDD
N	GND	GND	GND	GND	VDD	VDD	GND	GND	VDD	VDD
P	GND	GND	GND	GND	VDD	VDD	GND	GND	VDD	VDD
R	GND	VDDIO	VDDIO	GND	VDD	VDD	GND	GND	VDD	VDD
T	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
U	GND	GND	GND	FUSE_VQPS	RSVD	GND	GND	GND	AVDD_TS	GND
V	FLASH_DQ0	FLASH_DQ1	FLASH_RESET	VDD	GND	VDD	VDDIO	GND	GND	VDD
W	FLASH_SCLK	FLASH_DQ3	FLASH_CS1_N	RSVD	NC	NC	NC	NC	NC	NC
Y	GND	FLASH_DQ2	FLASH_CS0_N	RSVD	NC	NC	NC	NC	NC	NC

11	12	13	14	15	16	17	18	19	20	
PCIE_RX2_P	PCIE_TX2_P	PCIE_RX3_P	PCIE_TX3_P	GND	PCIE_AVDD_C	NC	I2C1_SCL	nRESET	GND	A
PCIE_RX2_N	PCIE_TX2_N	PCIE_RX3_N	PCIE_TX3_N	GND	PCIE_AVDD_C	NC	I2C1_SDA	JTAG_TCK	JTAG_TMS	B
GND	PCIE_AVDD_D	PCIE_AVDD_D	PCIE_AVDD_D	GND	GND	NC	I2C0_SCL	JTAG_TDO	JTAG_TDI	C
PCIE_CMN_REXT	GND	PCIE_AVDD_H	GND	GND	GND	IO_BS0	I2C0_SDA	CLK_IN	JTAG_TRSTN	D
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	E
GND	GND	VDD	VDD	GND	NC	NC	NC	NC	NC	F
GND	GND	VDD	VDD	GND	NC	NC	NC	NC	NC	G
GND	GND	VDD	VDD	GND	GND	VDDIO	VDDIO	VDD	VDD	H
GND	GND	PLL_AVDD	VDD	GND	GND	GND	GND	GND	GND	J
GND	GND	PLL_AVSS	VDD	GND	NC	NC	NC	NC	NC	K
GND	GND	VDD	VDD	VDD_SENSE1	NC	NC	NC	NC	NC	L
GND	GND	VDD	VDD	GND	VDDIO	VDDIO	GND	VDD	VDD	M
GND	GND	VDD	VDD	GND	GPIO_1	GND	GPIO_4	GND	GND	N
GND	GND	VDD	VDD	GND	GPIO_0	GPIO_3	GPIO_6	GPIO_7	NC	P
GND	GND	VDD	VDD	GND	GPIO_8	GPIO_9	GPIO_15	GPIO_26	GPIO_27	R
GND	GND	GND	GND	GND	GPIO_5	GPIO_10	GPIO_16	GPIO_25	GPIO_28	T
GND	GND	GND	GND	GPIO_2	GND	GPIO_11	GPIO_17	GPIO_24	GPIO_29	U
GND	VDD	VDDIO	GND	GND	VDD	GPIO_12	GPIO_18	GPIO_23	GPIO_30	V
NC	NC	NC	NC	GND	VDD	GPIO_13	GPIO_19	GPIO_22	GPIO_31	W
NC	NC	NC	NC	GND	GND	GPIO_14	GPIO_20	GPIO_21	GND	Y

Figure 3. Pin charts displaying the Hailo-8L ball chart pin assignments

2.2. Functional Assignment

Hailo-8L functional pin assignment is described below in Table 4

Pin Types are categorized as follows:

- Power - power rails
- I - input signals (Analog/LVCMOS)
- O - output signals (Analog/LVCMOS)
- OD - Open Drain IO

Table 4. Hailo-8L functional pin assignment

Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
Main Power and Sensing							
A01, A05, A15, A20, B05, B15, C04, C05, C09, C10, C11, C15, C16, D01, D04, D05, D07, D10, D12, D14, D15, D16, E04, E05, E06, E07, E08, E09, E11, E12, E13, E14, E15, E16, E17, E18, E19, E20, F04, F07, F08, F11, F12, F15, G01, G02, G03, G04, G07, G08, G11, G12, G15, H04, H07, H08, H11, H12, H15, H16, J07, J08, J11, J12, J15, J16, J17, J18, J19, J20, K02,	GND		Digital ground for device		Power		

Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
K04, K07, K08, K11, K12, K15, L02, L07, L08, L11, L12, M01, M02, M03, M04, M07, M08, M11, M12, M15, M18, N01, N02, N03, N04, N07, N08, N11, N12, N15, N17, N19, N20, P01, P02, P03, P04, P07, P08, P11, P12, P15, R01, R04, R07, R08, R11, R12, R15, T01, T02, T03, T04, T05, T06, T07, T08, T09, T10, T11, T12, T13, T14, T15, U01, U02, U03, U06, U07, U08, U10, U11, U12, U13, U14, U16, V05, V08, V09, V11, V14, V15, W15, Y01, Y15, Y16, Y20	GND		Digital ground for device		Power		
F05, F06, F09, F10, F13, F14, G05, G06, G09, G10, G13, G14, H05, H06, H09, H10, H13, H14, H19, H20, M19, M20, J05, J06, J14, K05, K06, K14, L05, L06, L09, L10, L13, L14, M05, M06, M09, M10, M13, M14, N05, N06, N09, N10, N13, N14, P05, P06, P09, P10, P13, P14, R05, R06, R09, R10, R13, R14, V04, V06, V10, V12, V16, W16	VDD		Digital supply		Power		
D02, D03, H17, H18, J09, J10, K09, K10, M16, M17, R02, R03, V07, V13	VDDIO		Digital supply for IO pads		Power		

Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
K13	PLL_VSSA		Analog ground for PLL		Power		
J13	PLL_VDDA		Analog supply for PLL		Power		
E10, U9	AVDD_TS		Analog supply for temperature sensor		Power		
L04	AVDD_VS		Analog supply for voltage sensor		Power		
J04	VDD_SENSE		Sense for VDD		Sensing		
L15	VDD_SENSE1		Sense for VDD		Sensing		
PCI Express (PCIe) Interfaces							
D06	PCIE_WAKE_N	Input	PCIe wake signal to host		LVCMOS		
D08	PCIE_CLKREQ_N	Output	PCIe clock request to host	Drive 0	LVCMOS		
D09	PCIE_PERST_N	Input	PCIe reset in	PD	LVCMOS	Yes	
D11	PCIE_CMN_REXT	I	PCIe calibration connection to external resistor		Analog		
A06, A08, A12, A14	PCIE_TX[0:3]_P	I	PCIe positive signal of data transmit diff-pair		Analog		
B06, B08, B12, B14	PCIE_TX[0:3]_N	O	PCIe negative signal of data transmit diff-pair		Analog		
A07, A09, A11, A13	PCIE_RX[0:3]_P	I	PCIe positive signal of the data receive diff-pair		Analog		
B07, B09, B11, B13	PCIE_RX[0:3]_N	I	PCIe negative signal of data receive diff-pair		Analog		
B10	PCIE_REFCLK_N	I	PCIe ref clock in negative		Analog		
A10	PCIE_ REFCLK_P	I	PCIe ref clock in positive		Analog		

Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
A04, A16, B4, B16	PCIE_AVDD_C		Analog power for high-speed clock and digital functions		Power		
C06, C07, C08, C12, C13, C14	PCIE_AVDD_D		Clean analog power for high speed clock		Power		
D13	PCIE_AVDD_H		PCIe Analog I/O voltage		Power		
Flash Interface							
V03	FLASH_RESET	Output	Flash reset out	PD, Drive 1	LVCMOS		
Y03, W03	FLASH_CS[0:1]_N	Output	Flash chip select, active low	PU, Drive 1	LVCMOS		
Pin multiplexed with GPIOs	FLASH_CS[2:3]_N		Flash chip select, active low	PD			
V01, V02, Y02, W02	FLASH_DQ[0:3]	Input	Flash data in/out		LVCMOS		
W01	FLASH_SCLK	Output	Flash clock	Drive 0	LVCMOS		
Universal Asynchronous Receiver Transmitter (UART) Interface							
J01, J02	UART[0:1]_RXD	Input	UART receive data	PD	LVCMOS	Yes	
H01	UART[0]_TXD	Input	UART transmit data	PD	LVCMOS	Yes	
H02	UART[1]_TXD	HiZ	UART transmit data		LVCMOS		
Inter-Integrated Circuit (I2C) Interface							
D18, B18	I2C[0:1]_SDA	Input	I2C[0-1] serial data	PU	LVCMOS		
C18, A18	I2C[0:1]_SCL	Input	I2C[0-1] clock	PU	LVCMOS		
Pin multiplexed with GPIOs	I2C[0:3]_ CURRENT_	I/O	Fast mode I2C pin				
SRC_EN							

Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
Pin multiplexed with GPIOs	I2C[2:3]_SDA	I/O	I2C[2-3] serial data				
Pin multiplexed with GPIOs	I2C[2:3]_SCL	O	I2C[2-3] clock				
Bootstrap							
D17	IO_BS0	Input	See Section 5.2.	PD	LVCMOS		
Reset and Clock							
D19	CLK_IN	Input	Main clock		LVCMOS		
A19	NRESET	I	Chip reset, active low	PD	LVCMOS	Yes	
JTAG							
C20	JTAG_TDI	Input	JTAG data input	PU	LVCMOS		
C19	JTAG_TDO	Output	JTAG data output	Drive0, PD	LVCMOS		
B20	JTAG_TMS	Input	JTAG mode select	PU	LVCMOS		
B19	JTAG_TCK	Input	JTAG clock	PD	LVCMOS		
D20	JTAG_TRSTN	Input	JTAG reset. Active low	PD	LVCMOS	Yes	
GPIO							
P16, U15, P17, N18	GPIO[0, 2-4]	Output	General configurable pins. Output during Bootup.	Drive 0	LVCMOS		
N16	GPIO[1]	Output	General configurable pins. Output during Bootup.	Drive X	LVCMOS		
T16	GPIO[5]	Output	General configurable pins. Output during Bootup.	Drive 1	LVCMOS		

Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
P18, P19, R16, R17, V17, W17, Y17, R18, T18, U18, V18, W18, Y18, Y19, W19, V19	GPIO[6-9, 12-23]	Intput	General configurable pins	PD	LVCMOS		
T17, U17, U19, T19, R19, R20, T20, U20	GPIO[10-11, 24-29]	Output	General configurable pins	Drive 0	LVCMOS		
V20, W20	GPIO[30-31]	Output	General configurable pins	Drive 1	LVCMOS		
Electronic Trace Management (ETM)							
Pin multiplexed with GPIOs	ETM_TRACE_CLOCK		ETM clock out				
Pin multiplexed with GPIOs	ETM_DATA[0-3]		ETM trace data out				
Miscellaneous							
H03, J03, U05, W04, Y04	RESERVED	I	Factory use only. Do not connect.	PD			
U04	FUSE_VQPS	I	Factory use only. Connect to GND.	PD			

3. Thermal Characteristics

3.1. Thermal Resistance

Package thermal resistance values for various junctions and airflow conditions are provided in Table 5.

The measurements were obtained using a JEDEC standard test board as defined in JESD51-9: Test Board for Array Surface Mount Package Thermal Measurements.

The JEDEC test board used for these results is characterized as follows:

- 8 layer PCB
- PCB dimensions - 101.5 mm x 114.5 mm
- PCB thickness - 1.6 mm

Table 5 Hailo-8L Thermal resistance

Location	Airflow	Thermal Resistance (° C/W)
Junction to ambient θ_{JA}_0	No airflow	8.9
Junction to ambient θ_{JA}_1	1 m/s airflow	7.8
Junction to ambient θ_{JA}_2	2 m/s airflow	7.3
Junction to board θ_{JB}	No airflow	2.28
Junction to case θ_{JC}	No airflow	0.35

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Stresses above the absolute maximum ratings listed in Table 6 and Table 7 may cause permanent damage to the device and affect device reliability. These values are stress ratings only; functional operation of the device under these conditions is not guaranteed or implied.

4.1.1. Power Rails

Table 6 provides the absolute maximum ratings of the power rails.

Table 6. Absolute maximum power rail ratings

Supply Name	Description	Min	Max	Unit
Digital Power Rails				
VDD	Top logic	-0.5	1.05	V
VDDIO	IO banks	-0.5	2.5	V
PCIe Analog Power Rails				
PCIE_AVDD_D	Analog power for non-high-speed clock and digital functions	-0.35	1.05	V
PCIE_AVDD_C	Clean analog power for high-speed clock applications	-0.35	1.05	V
PCIE_AVDD_H	High voltage power for the bias and parts of the PLL	-0.35	2.5	V
Miscellaneous				
PLL_AVDD	PLL analog power rail	-0.35	1.05	V
FUSE_VQPS	Factory use only. Connect to GND	-	-	V
AVDD_TS	Temperature sensor analog power rail	-0.35	2.5	V
AVDD_VS	Voltage sensor analog power rail	-0.35	2.5	V
Input voltage applied to digital IOs	Input Low Voltage	-0.35	2.5	V
V_ESD (HBM)	Electrostatic discharge voltage (Human Body Model)	2000		V
V_ESD (CDM)	Electrostatic discharge voltage (Charged Device Model)	500		V
Latch UP (LU)	Class II of JESD78E immunity level	A[1]		V

4.1.2. Thermal Ratings

Table 7 provides the storage and maximum junction temperature values.

Table 7. Absolute maximum thermal ratings

Parameter	Description	Value	Unit
T_Storage	Storage temperature	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

[1] Immunity level A: Pass the ±100mA and 1.5xVdd or MSV

4.2. Recommended Operating Conditions

Table 8 describes the recommended operating conditions for power rails, clocks, and ambient temperature.

Table 8. Hailo-8L operating ranges

Supply Name	Description	Min	Nom	Max	Unit
Digital Domain Power Rails					
VDD	Digital supply for core	0.78	0.83	0.88	V
VDDIO	Digital Power Rail for IO banks	1.62	1.8	1.98	V
PCIe PHY Analog Power Rails					
PCIE_AVDD_D	Analog power for non-high-speed clock and digital functions	0.78	0.83	0.88	V
PCIE_AVDD_C	Clean analog power for high-speed clock applications	0.78	0.83	0.88	V
PCIE_AVDD_H	High voltage power for the bias and parts of the PLL	1.08	1.8	1.98	V
Other Power Rails					
PLL_AVDD	PLL analog power rail	0.78	0.83	0.88	V
FUSE_VQPS	Factory use only -connect to GND	-	-	-	V
AVDD_TS	Temperature sensor analog power rail	1.62	1.8	1.98	V
AVDD_VS	Voltage sensor analog power rail	1.62	1.8	1.98	V
External Clocks					
CLK_IN [1]	Frequency	25±100PPM			MHz
	Duty Cycle	40	50	60	%
Ambient Operating Temperature					
T_A	Industrial grade	-40		85	^{o}C

[1] Connected to OSC_XIN clock pin, must receive a square wave clock signal (oscillator output clock signal)

4.3. Power-up Sequence

The power-up sequence should follow these guidelines[1]:

1. Initial state: nRESET pin is asserted (held low).
2. The VDDIO rises to 1.8V. Slew rate should be less than 18V/ms[2].
3. The VDD rises to 0.83V. VDD must hold VDD <VDDIO-0.3V. Slew rate of VDD should be less than 18V/ms.
4. PLL_VDDA should rise with VDD and be powered from VDD power regulator with filtering.
5. After the VDD reaches final level:
   a. Power-up PCIE_AVDD_D, PCIE_AVDD_C, PCIE_AVDD_H in any order. There are no timing limitations (minimum or maximum) when powering up multiple power supplies.
   b. PCIE_AVDD_D, PCIE_AVDD_C can be powered from VDD power regulator as long as noise target is met[3].
6. Enable reference clock after VDDIO has reached the final voltage level.
7. De-assert nRESET after clock is stable for 10 cycles. The clock is stable when it meets the requirements for CLK_IN.
8. For PCIe application: De-assert nRESET before or up to 500us PCIe PERST is de-asserted.
   For non-PCIe application: Add 1K-2K PU on PERSTn

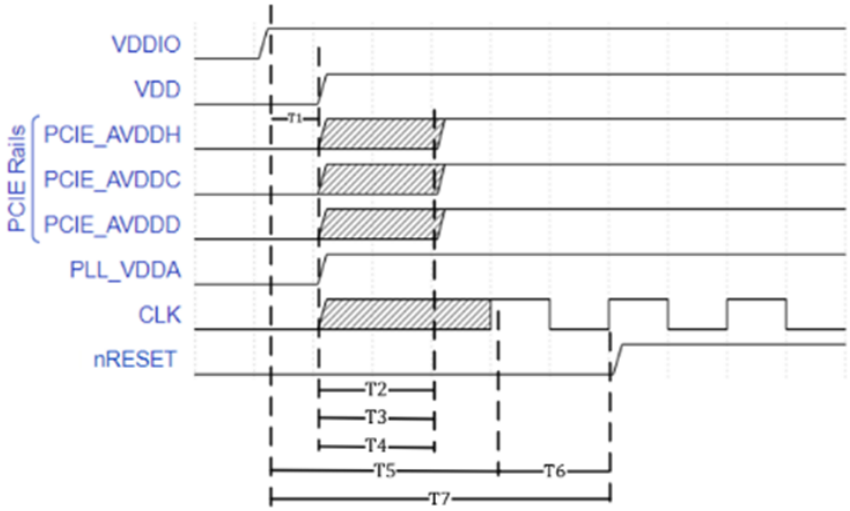

Figure 4 Hailo 8L Power-up sequence

[1]T12 requirement derived from PCI Express Specification Rev 3.0, Section 2.6.2. AC Specifications: T12 requirement derived from PCI Express Specification Rev 3.0, Section 2.6.2. AC Specifications:

Symbol	Parameter	Min	Max	Units	Notes
T_{PVPERL}	Power stable to PERST# inactive	100		ms	1

[2]"De-asserted NRESET such having enough margin to the end point enter LTSSM Detect State within 20 ms of the end of Fundamental Reset (PERSTn) , and 100ms before system sending a Configuration Request to the device".
[3]Refer to Table 9 and Table 10 and Section 4.8. for additional timing requirements.

Table 9. Power-up Sequence Timing Requirements

	Description	Min	Nom	Max	Unit	
T1	VDDIO to VDD	1	-	-	us	
T2	VDD to PCIE_AVDD_H	1	-	-	us	
T3	VDD to PCIE_AVDD_C	1	-	-	us	
T4	VDD to PCIE_AVDD_D	1	-	-	us	
T5	VDDIO to Stable Clock	1	-	-	us	
T6	Stable CLK to nRESET de-assertion	100	-	-	us	
T7	VDDIO to nRESET de-assertion	1	-	70	ms	For non-PCIe implementation
		1	-	PERST#	ms	For PCIe implementation

4.4. Power-Down Sequence

The power down sequence should follow the reverse order of the power up sequence.

1. Assert nRESET
2. Power down I/F power rails : PCIE_AVDD_D, PCIE_AVDD_C and PCIE_AVDD_H in any order.
3. Power down VDD and PLL_VDDA
4. De-assert reference clock before VDDIO power-down.
5. Power down the VDDIO

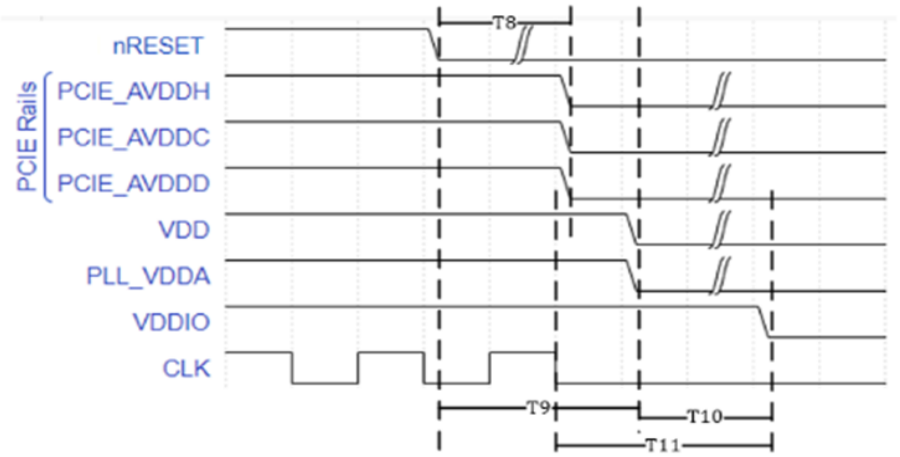

Table 10. Power-Down Sequence Timing Requirements

	Description	Min	Nom	Max	Unit
T8	nRESET assertion to PCIE power rails power down	1	-	-	us
T9	nRESET assertion to VDD power down	1	-	-	us
T10	VDD to VDDIO power down	1	-	-	us
T11	CLK De-assertion to VDDIO power down	1	-	-	us

4.5. Power Consumption

4.5.1. Maximum Supply Current

The maximum current that can be drawn from each power rail is application dependent. The measurements in Table 11 were made during device characterization and represent worst-case results across all PVT corners. The numbers are provided here only as general guidelines for power supply design.

Table 11. Maximum supply current

Supply Name	*Max Current	Unit
VDD[1]	14.5	A
VDDIO[2]	0.3	A
PCIE_AVDD_D	280	mA
PCIE_AVDD_C	180	mA
PCIE_AVDD_H	21	uA
PLL_AVDD	1.2	mA
AVDD_TS	0.5	mA
AVDD_VS	0.3	mA

4.5.2. Supply Current in Selected Test Cases

To illustrate how power consumption depends on the compute intensity, Table 12 presents the Hailo-8L average power under selected test cases. Measurements were taken at an ambient temperature of 25°C with VDD set to 0.8V while the Hailo-8L was operating in normal power mode.

Table 12. Power consumption

Test Condition	Average Power	Comments
[3]**Model: Resnet50** 500 FPS	1.9W	batch=8
Model: YOLOv8m 87 FPS	3.14W	batch=8
Model: YOLOv11m 58 FPS	2.2W	batch=8

[1]The maximum current assumes heavy compute networks, for lowering the values, if needed, please evaluate the specific neural model and Hailo-8L integration for the specific network and add an adequate margin to cover all PVT corners and current spikes.

[2] $VDDIO[V] \cdot \sum_{IO_i}\left(C_i[F] \cdot \frac{1}{2} \cdot f_{switching}[Hz]\right)$ Each IO_i drives a capacitance C_i[F] and is switched from 1 to 0 and vice versa at a frequency of 0.5f[Hz]. Add C_i[F]x0.5f[Hz] of all the IOs and multiply this sum by the VDDIO [V] voltage rail to obtain the VDDIO current consumption
I_VDDIO[A].

[3]The models were compiled using the Hailo Software Suite, and inference was executed using HailoRT.

4.6. Digital I/O DC Characteristics

There are two types of digital of I/O:

1. **Failsafe I/Os with strong pull-up or pull-down**
   Signals in this group are: PCIE_PERST_N, PCIE_CLKREQ_N, PCIE_WAKE_N, GPIO0, GPIO1, CLK_IN and NRESET.
2. **Regular I/Os**: All remaining GPIOs use this I/O type.

Table 13 describes the DC characteristics of the failsafe digital pins as characterized across all PVT corners.

Table 13. Failsafe digital pin DC characteristics

Symbol	Parameter	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage	-0.3		0.35*VDDIO	V
V_{IH}	Input High Voltage	0.65*VDDIO		1.98	V
V_{T}	Threshold Point	0.91	1	1.13	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	0.97	1.09	1.2	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	0.75	0.86	0.97	V
V_{TPU}	Threshold point with Pull-Up Resistor Enabled	0.82	0.95	1.07	V
V_{TPD}	Threshold point with Pull-Down Resistor Enabled	0.91	1.01	1.14	V
V_{T+PU}	Schmitt Trigger Low to High Threshold Point with Pull-Up Resistor Enabled	0.87	1	1.13	V
V_{T-PU}	Schmitt Trigger High to Low Threshold Point with Pull-Up Resistor Enabled	0.69	0.8	0.92	V
V_{T+PD}	Schmitt Trigger Low to High Threshold Point with Pull-Down Resistor Enabled	0.98	1.09	1.22	V
V_{T-PD}	Schmitt Trigger High to Low Threshold Point with Pull-Down Resistor Enabled	0.75	0.86	0.98	V
I_{L}	Input Leakage Current @ Vi=1.8V or 0V			+/-10	uA
I_{OZ}	Tri-State Output Leakage Current @ Vi=1.8V or 0V			+/-10	uA

Symbol	Parameter	Min	Typical	Max	Unit
R_{PU}	Pull-Up Resistor	31	46	84	KΩ
R_{PD}	Pull-Down Resistor	31	44	71	KΩ
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
C	Output/Input capacitance	-	1.05	-	pF

Table 14 describes the DC characteristics of the regular GPIOs pins, as characterized across all PVT corners.

Table 14. Regular GPIOs DC characteristics

Symbol	Parameter	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage	-0.3		0.35*VDDIO	V
V_{IH}	Input High Voltage	0.65*VDDIO		1.98	V
V_T	Threshold Point	0.82	0.92	1	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	0.98	1.1	1.21	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	0.74	0.82	0.9	V
V_{TPU}	Threshold point with Pull-Up Resistor Enabled	0.82	0.91	1	V
V_{TPD}	Threshold point with Pull-Down Resistor Enabled	0.83	0.93	1.02	V
V_{T+PU}	Schmitt Trigger Low to High Threshold Point with Pull-Up Resistor Enabled	0.97	1.09	1.2	V
V_{T-PU}	Schmitt Trigger High to Low Threshold Point with Pull-Up Resistor Enabled	0.73	0.81	0.89	V
V_{T+PD}	Schmitt Trigger Low to High Threshold Point with Pull-Down Resistor Enabled	0.99	1.11	1.22	V
V_{T-PD}	Schmitt Trigger High to Low Threshold Point with Pull-Down Resistor Enabled	0.75	0.83	0.91	V
I_L	Input Leakage Current @ Vi=1.8V or 0V			+/-10	uA
I_{OZ}	Tri-State Output Leakage Current @ Vi=1.8V or 0V			+/-10	uA

Symbol	Parameter	Min	Typical	Max	Unit
R_{PU}	Pull-Up Resistor	17	24	40	KΩ
R_{PD}	Pull-Down Resistor	17	23	36	KΩ
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
C	Output/Input capacitance for all other pads	-	0.88	-	pF

4.7. PCIe Characteristics (DC and AC)

The following tables describe the PCIe characteristics as characterized across all PVT corners.

Table 15. PCIe Gen1 transmitter characteristics

Parameter	Description	Min	Max	Unit
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	876	1130	mV
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	489.33	669.19	mV
LTX-SKEW	Lane-to-Lane Output Skew	-	0.438	ns

Table 16. PCIe Gen2 transmitter characteristics

Parameter	Description	Min	Max	Unit
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	810	1070	mV
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	445	625	mV
LTX-SKEW	Lane-to-Lane Output Skew	-	0.235	ns

Table 17. PCIe Gen3 transmitter characteristics

Parameter	Description	Min	Max	Unit
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	800	1010	mV
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	401	547	mV
VTX-EIEOS-FS	Minimum voltage swing during EIEOS for full swing signaling	262	-	mVPP
VTX-EIEOS-RS	Minimum voltage swing during EIEOS for reduced swing signaling	256	-	mVPP
LTX-SKEW	Lane-to-Lane Output Skew	-	0.438	ns

Table 18. PCIe transmitter data rate independent characteristics

Parameter	Description	Min	Max	Unit
VTX-AC-CM-PP	Tx AC peak-peak common mode voltage	-	134	mVPP
VTX-DC-CM	Tx DC peak-peak common mode voltage	0.396	0.404	V
VTX-CM-DC-LINE-DELTA	Absolute Delta of DC Common Mode Voltage between D+ and D-	2.1	7.2	mV
VTX-IDLE-DIFF-AC-p	Electrical Idle Differential Peak Output Voltage	8.09	19.98	mV
VTX-IDLE-DIFF-DC	DC Electrical Idle Differential Output Voltage	0.1	1.4	mV
ZTX-DIFF-DC	DC differential Tx impedance	69.2	75.3	Ω

Table 19. PCIe receiver electrical idle detect threshold

Parameter	Description	Min	Max	Unit
VRX-IDLE-DET-DIFF-PP	Electrical Idle Detect threshold	92	154	mV

Table 20. PCIe receiver termination characteristics

Parameter	Description	Min	Max	Unit
ZRX-DC	Receiver DC single ended impedance	49.7	54.9	Ω
ZRX-HIGH-IMP-DC-POS (0-200 mV)	DC input CM input impedance for V≥0 during Reset or power-down	53k	-	Ω
ZRX-HIGH-IMP-DC-POS (> 200 mV)	DC input CM input impedance for V≥0 during Reset or power-down	144k	-	Ω
ZRX-HIGH-IMP-DC-NEG	DC input CM input impedance for V<0 during Reset or power-down	4.6k	-	Ω

4.8. Reset Timing Characteristics

The NRESET pad should be driven with a reset signal that meets the timing requirements described below to ensure a valid reset pulse for the Hailo-8L device:

1. Rise and fall time (measured between 20% and 80% of VDDIO) < 5ns
2. NRESET assertion time (held low) >28us.

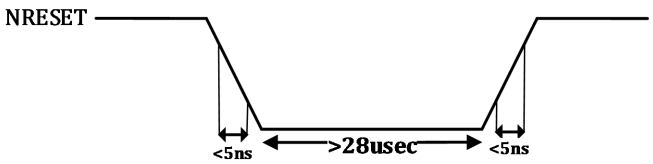

Figure 5. Reset Characteristics

5. Detailed Description

This section describes the main system mode and usage scenario for the Hailo-8L device and provides supporting information on its subsystems.

For additional details, refer to the Hailo-8L software documentation available on the Hailo Developer Zone.

5.1. System Modes and Usage

In the primary usage mode, shown in Figure 6 Hailo-8L operates as a companion device that offloads neural network workloads from the host processor. The device receives inference data, processes it efficiently, and returns the results, typically communicating with the host processor over PCIe

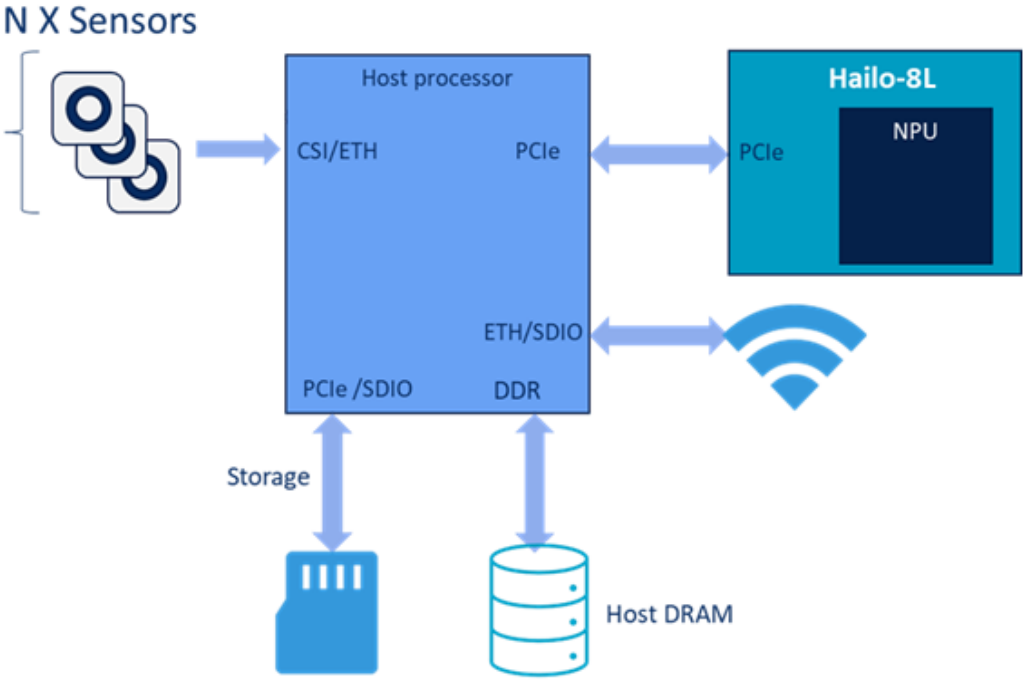

Figure 6. Hailo-8L as a Companion Device

5.2. Bootstraps

Hailo-8L includes one functional bootstrap, IO_BS0, which selects between two possible boot modes: PCIe boot when the bootstrap is pulled up, or Flash boot when it is pulled down.

- PCIe boot: The Hailo-8L ROM manages the boot process in coordination with the host processor running the HailoRT PCIe driver. The Hailo-8L firmware is then fetched over the PCIe link to complete device initialization.
- Flash boot: The Hailo-8L ROM loads its firmware directly from an SPI flash device to complete the boot process.

Appropriate boot flow may be selected based on specific system requirements.
Refer to the flow diagram in Section 5. for further details.

For further implementation guidance and bootstrap connectivity recommendations, see the Hailo-8L Hardware Integration Guide.

5.3. NN Core

The Hailo-8L NN Core enables efficient deployment of Deep NNs (DNNs) using eight internal functional units called clusters.

Key features include:

- Up to 13 TOPs at 8-bit precision
- Four clusters that support deployment of multiple NNs.
  - Compute, control and memory structure optimized for NN primitives.
  - Fully programmable architecture supporting all common NN building blocks through the Hailo Dataflow Compiler (this includes, but is not limited to, layers such as convolution, pooling, fully connected and activation).
  - Native support for advanced NN architectures, including split, concatenation and add layers.
- Power modes
  - Power shutdown available at cluster level
- Up to 16 I/O channels to the NN core
- Configurable interconnect between NN core inputs, outputs and pre/post units.
- 8/16-bit precision for both weights and activations, configurable at layer granularity.
- 4-bit precision for weights, configurable at layer granularity.
- NN pre/post processing hardware accelerator used to offload the following functions from host:
  - Up to eight pre/post processing configurable engines
  - NMS engine
    - Up to 128k proposals post score threshold
    - One comparison per cycle, two NMS engines may be aggregated to offer double throughput
    - Configurable intersection over union and score threshold with up to 16 threshold classes
  - Bilinear interpolation engine
    - Streaming bilinear up to 8K resolution
    - Crop and Resize operations
  - Reshape engine
    - Translates standardized formats to Hailo proprietary format and vice versa
    - Offloads advanced tensor reshape operations
  - Softmax engine

5.4. High Bandwidth Interfaces

5.4.1. PCI Express (PCIe)

Hailo-8L includes a PCI-SIG compliant 4-lane PCIe Gen3 PHY and controller, enabling integration as a PCIe endpoint. It provides a dedicated scatter-gather DMA for efficient memory mapped transactions.

Key features include:

- Up to 32 Gbps bi-directional throughput
  - x1, x2, x4 lane configurations
  - Supports link rate of 2.5, 5.0, 8.0 GT/s per lane
- Lane reversal support
- L1 PM Sub-states with CLKREQ
- Latency Tolerance Reporting (LTR)
- Single Physical Function
- Single Virtual Function
- Single Virtual Channel (VC)
- Up to 2.5µs read latency from host memory in full BW
- Support also Device low power modes - D0, D3
- Up to 256 Byte maximum payload size
- Advanced Error Reporting (AER) support
- ECRC generation and check support
- MSI (up to 32) and INT message support
- Internal DMA (32 channels)
- Dynamic Scatter-Gather DMA configuration, such as interrupt generation or start and end conditions for each specific SG page.
- Core Context switch over PCIe – configuration and data
- FW boot from PCIe
- Control protocol
- Up to 16 dedicated RX and TX channels with low latency streaming FIFOs
- Supports out of order TLP arrival with integrated re-order buffer
- Retransmit buffer of 2KB
- Receive buffer of 2KB
- Up to 32 outstanding read requests
- Integrated safety mechanisms that detect transient and permanent faults in data and control

paths

- Full support for link power management including ASPM L0, ASPM L1, L1.1 and L1.2

5.5. Low Bandwidth Interfaces

5.5.1. Inter-Integrated Circuit (I2C)

Hailo-8L includes up to four I2C interfaces that may also operate as SCCB (Serial Camera Control Bus) masters for sensor control.

Key features include:

- Each interface can operate as Master or Slave
- Supports high-speed and low-speed modes
- Bandwidth options
  - Fast mode, up to 400Kbps
  - High-speed mode, up to 3.4Mb/s

5.5.2. Quad Serial Peripheral Interface (QSPI)

Hailo-8L includes a single QSPI interface for connection to external Flash devices.

Key features include:

- Supports up to two external Chip Selects (CS)
- Execute in Place (XIP) capability
- Up to 1Gb external memory address space
- SPI (x1), DSPI (x2) and QSPI (x4) modes
- DDR and SDR modes
- Boot from external Flash
- External device clock frequency of up to 50MHz

5.5.3. Universal Asynchronous Receiver Transmitter (UART)

Hailo-8L includes two simple UART interfaces (UART0 and UART1) without flow-control signals.

Key features include:

- 8-bit communication with parity and fixed at one stop bit
- Baud rate up to 2Mbaud

5.6. MCU

Hailo-8L includes two ARM® Cortex-M4 processors with an associated memory subsystem. These processors are used exclusively by the Hailo-8L firmware and are not available for any other purpose

5.6.1. ARM Cortex M4 Processors

Each of the two ARM Cortex-M4 processors are equipped with a Memory Protection Unit (MPU) and a Floating Point Accelerator Unit (FPU) engine.

The processors communicate with each other through mailbox and semaphore modules.

Key features include:

- MPU
- FPU
- Embedded Trace Microcell (ETM)
- Support for up to 200MHz frequency
- ARM processor based on ARMv7 architecture
- Boot from external Flash or PCIe by external boot strap pins

5.6.2. MCU Memory

The MCU memory is accessible by both processors.

Key features include:

- Six data/code memory ports
- Total of 640KB SRAM memory for code and data with ECC
- 128KB ROM
- Up to 1Gb memory space for external Flash devices

5.6.3. Flash System

The Hailo-8L flash system is based on external serial Flash devices connected through the QSPI controller. External Flash is typically used to store firmware and application code for the MCU subsystem. Software can either execute directly from serial Flash using execute-in-place (XIP) or copy code and data into internal SRAM, according to system requirements.

Key features include:

- Integration with the QSPI controller for external Flash access
- Support for execute-in-place (XIP) from external serial Flash
- Use of external non-volatile memory for firmware and application storage

5.7. System Peripherals

5.7.1. Temperature Sensor

The Hailo-8L includes a high-precision low-power junction temperature sensor embedded in the chip. Typical uses include clock speed optimization, power management and thermal management.

Key features include:

- +/- 3.0°C accuracy
- 12-bit resolution (10-bit and 8-bit alternatives at lower accuracy), parallel or serial
- Signature response on demand
- Analog fault coverage

5.7.2. Voltage Monitor

Hailo-8L includes two on-chip voltage monitors that are low-power self-contained blocks designed to monitor differential voltage levels within the core logic voltage domains.

Key features include:

- 16 monitoring points
- +/-1% accuracy
- Up to 14-bit resolution
- Digital interface
- Signature response on demand
- Analog fault coverage

5.8. Security System

5.8.1. Features

Hailo-8L includes set of security features designed to support typical target applications.

The security subsystem includes:

- Secure boot
- Complete Life Cycle Management (LCM)
- User-provided non-volatile hash (enabling RoT behavior)
- User access to hardware-accelerated cryptographic algorithms
- Secure debug access according to the product life cycle
- Inner configurable firewall to block unexpected access to secure system regions

5.8.2. True Random Number Generator (TRNG)

Hailo-8L includes a TRNG that generates 32-bit random numbers using an integrated analog circuit.

The TRNG is fully compliant with FIPS 140-2.

5.8.3. Cryptographic Accelerator

Hailo-8L includes a hardware authentication engine and an encryption/decryption engine that support the following algorithms:

- AES (128,192,256)
- SHA1/2
- RSA (2048,3072,4096)

These accelerators can be used for secure boot, data-at-rest and data-in-transit.

5.8.4. Trusted Execution Environment (TEE)

The Hailo-8L TEE monitors and controls incoming and outgoing traffic inside the chip based on predetermined security rules set during software boot.

5.8.5. Firewall

The Hailo-8L includes a configurable hardware firewall that protects access to peripherals inside the device, internal SRAM regions, and external memory spaces.

The firewall enforces access control policies and strengthens the overall security posture of the system.